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A Diode Clamped Potential Balancing Method For Z-Source Diode Clamped Inverters by Using Shoot-Through Offset

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A B S T R A C T

Conventional buck-boost three-level inverters are compared with the the Z-source Diode Clamped inverters have more simple structure with improved output waveform quality. But the diode point potential unbalance problem is still a drawback for their applications. Based on the research of SPWM modulation method and the analysis of the effect of the shoot-through states on the diode clamped potential, this paper proposes a diode clamped potential balancing method by adding the shoot-through offset which can be applied to the constant boost control and the third-harmonic-injection control. This new method is simple and has the advantage that the diode clamped potential unbalance problem can be improved with the high voltage gain, which is verified by simulation results.

KeyWords: Z-source； Diode clamped unbalanced problem ; shoot-through offset； SPWM.

1 INTRODUCTION

In recent years, multilevel inverters have been widely used in high-power and high-voltage applications, among which the three-level Diode Clamped inverter topology is applied most extensively [1]. For two-level inverters, an impedance-source inverter abbreviated as Z-source inverter (ZSI) is presented in [2]. As ZSI has buck-boost capability, it replaces the conventional inverter and simplifies the two-stage structure to a single-stage structure. Furthermore, ZSI improves system security because it allows the devices of each phase leg gated on simultaneously. To take advantage of three-level inverter,[3] and [4] combined Z-source with three -level inverter and presented dual Z-source three-level Diode Clamped inverter. This inverter consists of two dc power supplies, two Z-source impedance networks and the three-level Diode Clamped inverter circuit. Because of the Z-source network, the shoot-through mode become a special operating mode which can boost the dc input voltage, while avoiding the device destroy in the shoot-through state. This inverter need not set the dead time which can cause the waveform distortion. In short, compared to the conventional Diode Clamped inverter, it has several advantages. Instead of adopting the double-network circuitry directly without modification, an alternative topology is presented in[5] that used only one Z-source impedance network at a significantly reduced cost but can achieve the same effect. In the applications of the single-supply operation, the inverter which was presented in [4] cannot be applied because it needs two dc power supplies. To overcome this limitation, two capacitors with the same capacitance in series can be used in parallel connecting to the single power supply which can replace the two dc power supplies approximately based on the capacitive divider principle [11]. The topology of Z-source three-level Diode Clamped inverter with single dc-source is shown in Fig.1. In this figure, Udc is the dc input voltage, C1 and C2 are two divider capacitors with the same capacitance（C1=C2）,O is the mid-point. Diodes D1 and D2 are conductive in the none shoot-through state，but turn off in the shoot-through state. The Z-source impendence network consists of two capacitors (Cz1 and Cz2) and two inductances (Lz1 and Lz2) connected in an X fashion.

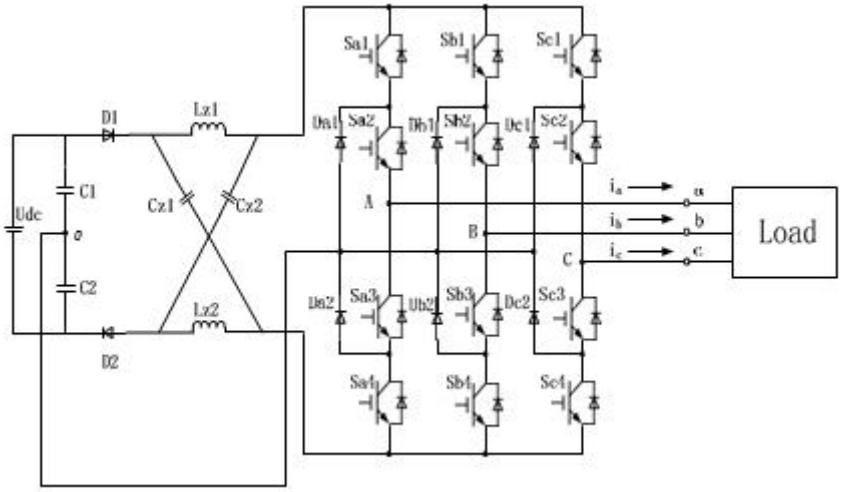

Fig.1 Z-source three-level Diode Clamped inverter with a dc-source

However, the diode clamped potential unbalance problem is an internal problem of 3-level Diode Clamped inverter which is also consisted in the Z-source Diode Clamped inverter. To the Z-source Diode Clamped inverter, this is an urgent issue because it will increase the harmonic distortion of the output waveform and the voltage stresses of switching devices, and even destroy the switching devices or the capacitors. To overcome this drawback, this paper presents a neutral-point potential balancing method by adding the shoot-through offset. Firstly, this paper introduces the switching states of Z-source Diode Clamped inverter and the principle of SPWM control method. Secondly, it introduces two carrier-based PWM methods which can produce different shoot-through states and analysis the effect of different shoot-through to the neutral-point potential. Thirdly, it calculates the shoot-through offset and combines the offset with the SPWM control method to improve the neutral-point potential unbalance problem.

2.Switching States of Z Source Diode Clamped Inverter and SPWM Control Method

The Z-source three-level Diode Clamped inverter advantageously utilizes the shoot-through states to boost the dc bus voltage by gating on the upper two switches and the lower two switches of a phase leg. Therefore, in addition to the valid states and zero state, the Z-source Diode Clamped inverter has several unique shoot-through states. Tab.1 lists the status of the switches of phase A leg and the corresponding output voltage [6]. It can be seen that the Z-source Diode Clamped inverter has three shoot-through states: full shoot-through state(Full-ST), upper shoot-through state(Upper-ST) and lower shoot-through state(Lower-ST).

Table I Switching States Of Z-Source Diode Clamped Inverter

State Type	ON Switches	ON Diodes	Va
Non-ST	Sa1,Sa2	D1,D2	Vi/2
Non-ST	Sa2,Sa3	D1,D2,Da1(or Da2)	0
Non-ST	Sa3,Sa4	D1,D2	-Vi/2
Full-ST	Sa1,Sa2,Sa3,Sa4	None	0
Full-ST	Sa1,Sa2,Sa3, Sc2,Sc3,Sc4	Da2,Dc1	0
Upper-ST	Sa1,Sa2,Sa3	Da2,D1	---
Lower-ST	Sa2,Sa3,Sa4	Da1,D2	---

For conventional Diode Clamped inverters, reference [9] has presented the two carrier-based PWM methods: Phase opposite disposition level-shifted PWM method (POD-LSPWM) and In-phase disposition level-shifted PWM method (IPD-LSPWM). Both of the methods use two level-shifted carrier signals and three reference signals generate the switching signals. The carrier signals of IPD method have the same phase while in the POD method, the carrier signals have the phase difference of π radians. It can be seen from Table 1, the Z-source Diode Clamped inverter hasthree shoot-through states: full shoot-through state, upper shoot-through state and lower shoot-through state. In essence, it is the carrier-based PWM method which is chosen for the Z-source Diode Clamped inverter decides the shoot-through state full shoot- through or not [10]. Fig.2 shows the POD-LSWM for Z-source Diode Clamped inverter. In this method, the upper shoot-

through signal compares with the upper carrier signal Vp to decide the position where the shoot-through state should be added into. The lower shoot-through signal Vn compares with the lower carrier in the same way. As the figure shows, the two shoot-through states are added into the same position which cause the switching device 1 and switching device 4 are gated on the same time. So the control signal of phase A leg is 1111, so the four switching devices are all gated on meanwhile and the Z-source Diode Clamped inverter in full shoot-through state right now.

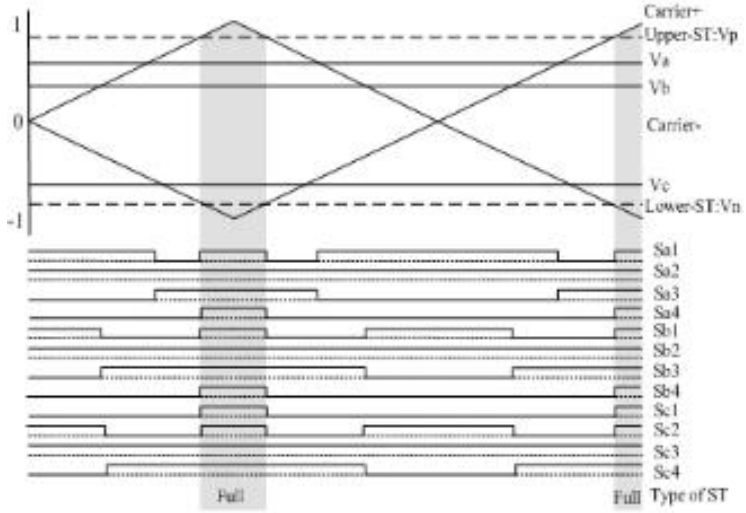

Fig.2 Phase opposite disposition level-shifted PWM method for Z-sourceDiode Clamped inverter.

Fig.3 shows the IPD-LSWM for Z-source Diode Clamped inverter. In this method, the upper shoot-through signal compares with the upper carrier signal Vp to decide the position where the shoot-through state is added into. The lower shoot-through signal Vn compares with the lower carrier in the same way. The two shoot-through states are added into different positions in one switching period So the control signal of phase A leg is 1110 or 0111, it means that there are only three switching devices gated on at the same time and the Z-source Diode Clamped inverter in upper shoot-through state or lower shoot-through state.

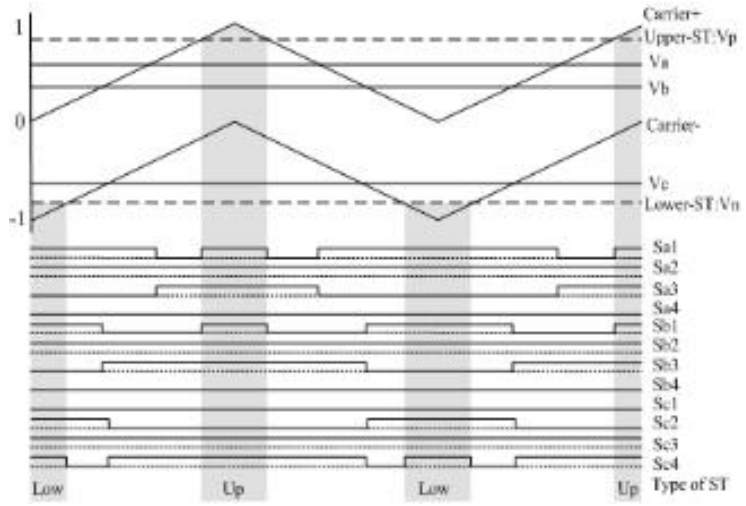

Fig.3 In-phase disposition level-shifted PWM method for Z-source Diode Clampedinverter

3.. New SPWM Control Method ForBalancing diode clamped Potential

The analysis of the shoot-through state and its effect tothe diode clamped

It is the unbalanced charging and discharging of C1 and C2 cause the diode clamped potential unbalance problem. If the Voltages of the two capacitors can be controlled almost the same, the unbalance problem will be improved to a great extent [12]. It can be seen from fig.4, in the full shoot-through state, the z-source network is separated with the dc input due to the reverse blocking action of diodes D1 and D2, so the discharging circuit cannot be formed for the capacitors C1 and C2. It means the full shoot-through state has no help in improving the neutral-point potential unbalance problem. Fig.5 and fig.6 shows that the discharging circuit of Capacitor C1 can be formed when the Z-source Diode Clamped inverter in upper shoot-through state and the discharging circuit of Capacitor C2 can be formed when in lower shoot-through state. Therefore, the voltage fall time can be postponed by postponing the upper shoot-through time, while the voltage of C1 drops at once. In the same way, the voltage of C2 will drop more when the lower shoot-through time postponed.

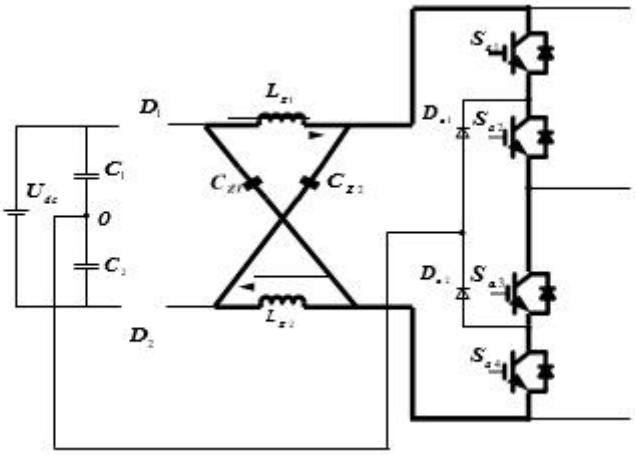

Fig.4 The current-loop of Z-source Diode Clamped inverter in full shoot-through state

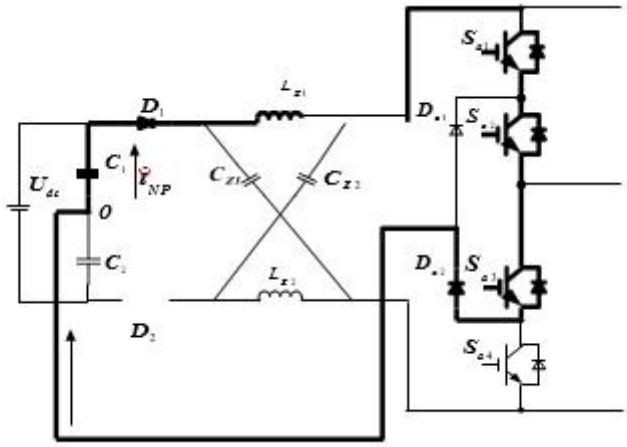

Fig.5 The capacitor discharging circuit of Z-source Diode Clamped inverter in uppershoot-through state

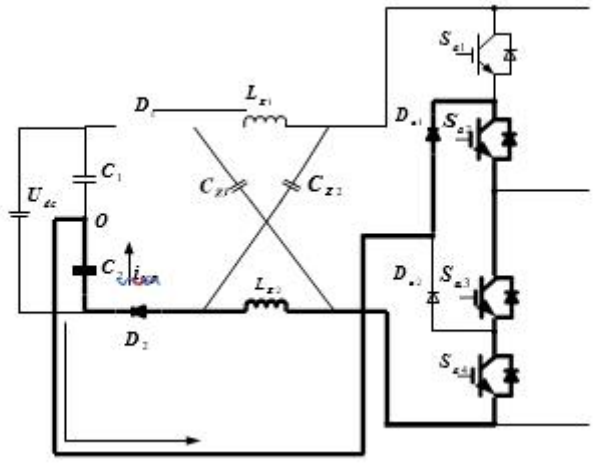

Fig.6 The capacitor discharging circuit of Z-source Diode Clamped inverter in lowershoot-through state

4.Simulation Results and Analysis

The Matlab/Simulink simulations have been carried out to verify the effectiveness of the SPWM control method with the shoot-through offset. The shoot-through offset is added into both the maximum constant boost control method and the third-harmonic-injection control method to improve the neutral-point potential unbalance problem. Tab.2 shows the simulation parameters in detail.

Table 2. The System Parameters Considered For Simulation

Parameters	Specification	Unit
DC Supply	200	V
Output Frequency	50	Hz
Switching Frequency	12k	Hz
Z-source Inductor	1	mH
Z-source Capacitors	300	uF
Load	10	Ω

Firstly, the conventional maximum constant boost control method is simulated by setting M = 0.7, d_0 = 0.3. Fig.8 shows the output waveforms of three-phase load, top to bottom are the output voltage of three-phase load, the output current of phase A leg and the line voltage. Fig.9 shows the fluctuation of diode clamped potential and the difference value of C_1 and C_2. In detail, neutral-point potential fluctuates between 99 and 101V, the U_C fluctuates between -2 and 1.6V. Fig.10 shows the total harmonic distortion (THD) of output current and line voltage are 0.96% and 44.57% respectively.

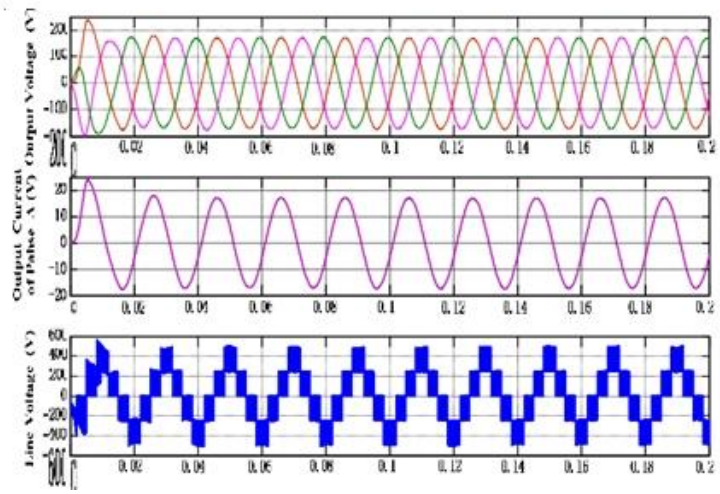

Fig.7 Simulation results of conventional maximum constant boost controlmethod for M=0.7, d0=0.3

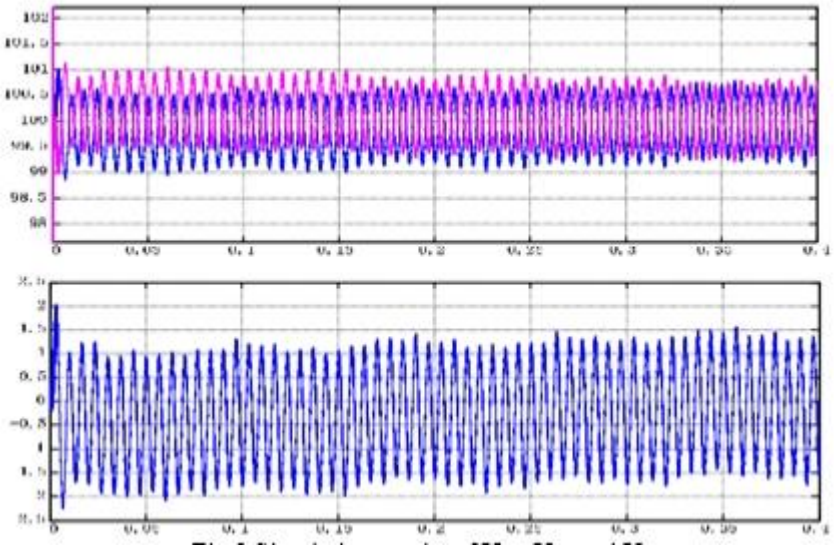

Fig8: Simulation results of UC1,UC2 and UC

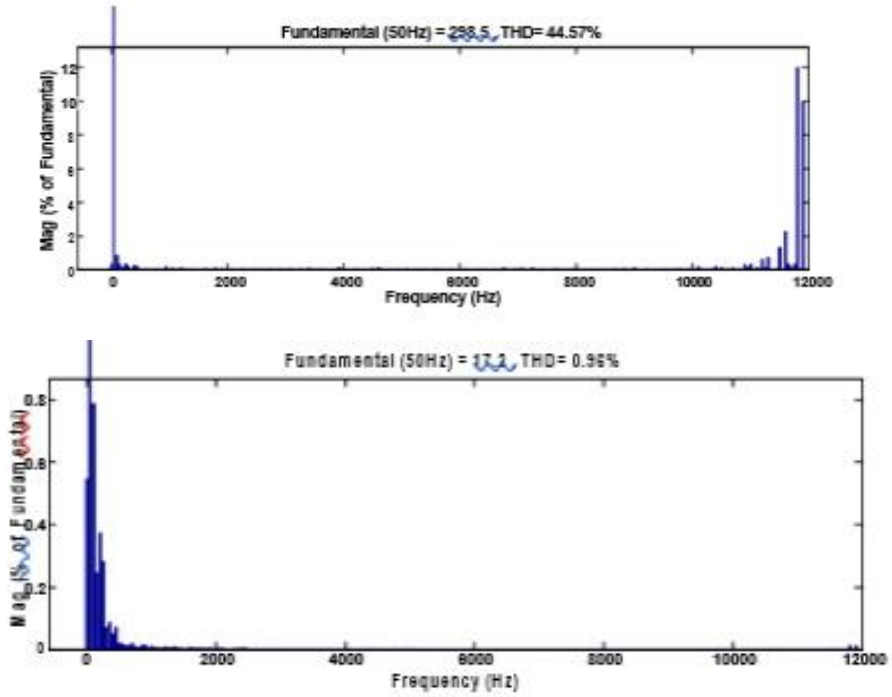

Fig.9 The THD of the output current and the line voltage

Then, the maximum constant boost control method with the shoot-through offset is simulated. Set M = 0.7, d_0 = 0.3, K=0.26. Fig.11 shows the output waveform of three-phase load, top to bottom are the output voltage of three-phase load, the output current of phase A leg and the line voltage. Fig.12 shows the fluctuation of neutral-point potential and the difference value of C_1 and C_2. In detail, neutral-point potential fluctuates between 99.8 and 100.2V, the U_C fluctuates between -0.4 and 0.4V. Fig.12shows the total harmonic distortion (THD) of output current and line voltage are 0.48% and 43.89% respectively

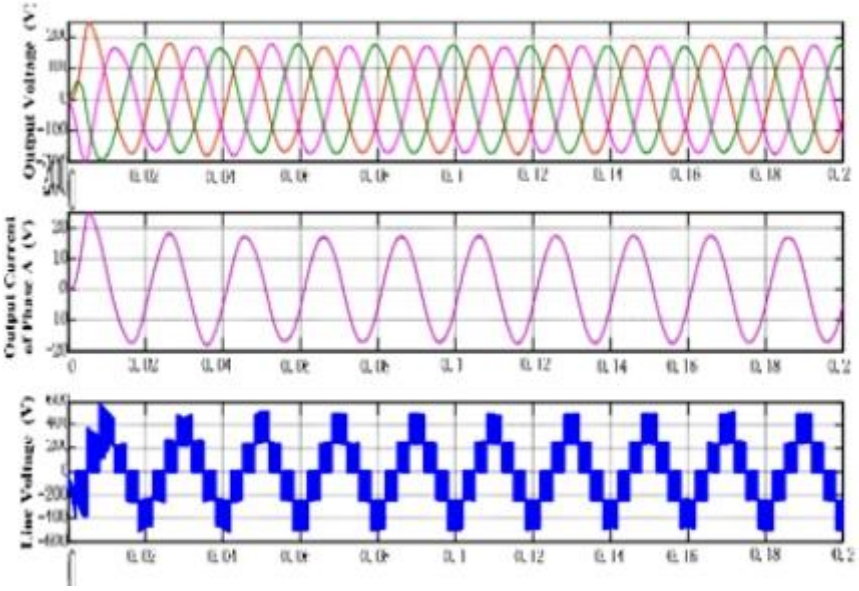

Fig.10 Simulation results of maximum constant boost control method withshoot-through offset for M=0.7, d0=0.3, K=0.26

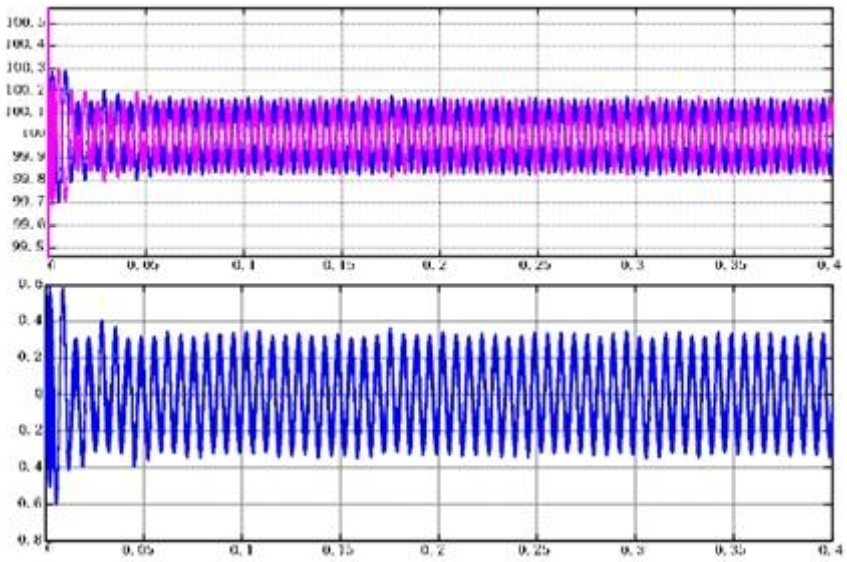

Fig.11 Simulation results of U_{C1}, U_{C2} and DU_C for K=0.26

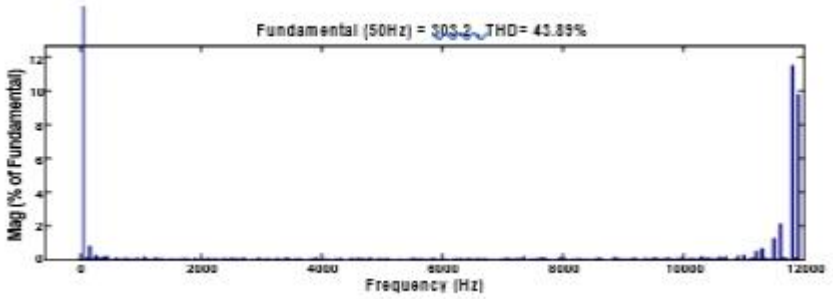

Fig.12 The THD of the output current and the line voltage for K=0.26

Compared these two different methods, the latter with the shoot-through offset can improve the diode clamped potential effectively and reduce the THD of the output current and the line voltage. Furthermore, the high voltage gain can be kept meanwhile.The shoot through offset can also be added into the third-harmonic-injection control to improve the diode clamped potential unbalance problem. The specific simulation results showed in Table 4.In order to research the effect of K, M, d_0 to the system in detail, the parameters are changed the value and the simulation results showed in Table 3 and Table 4

Table 3. The Parameters KMD Of The Maximum Constant BoostControl Method And The Output Waveform Quality

K	M	d0	Vout (V)	ΔUc (V)	THDu (%)	THDi (%)
0	0.7	0.3	172.8	-1.8~1.8	44.57	0.96
0.26	0.7	0.3	172.7	-0.32~0.3	43.89	0.48
0	0.6	0.42	351.3	-3.2~3.2	49.22	1.26
0.26	0.6	0.42	379.2	-1.2~1.2	49.09	0.93
0.42	0.6	0.42	389.4	-0.8~0.8	49.21	0.89

Table4 The Parameters KMD Of Third-Harmonic-InjectionControl Method And The Output Waveform Quality

K	M	d0	Vout (V)	ΔUc (V)	THDu (%)	THDi (%)
0	0.7	0.3	168.8	-0.8~0.8	44.44	053
0.26	0.7	0.3	173.7	0.2~0.2	44.04	0.26
0	0.6	0.42	363.5	-2~2	49.47	1.11
0.26	0.6	0.42	389.2	-0.9~0.9	49.72	0.98
0.42	0.6	0.42	382.5	-0.8~0.8	49.39	0.7

Table 3 and Table 4 show that increasing the K value can reduce the U_C which caused by the diode clamped potential unbalance problem. When the modulation index M is constant, the K and d_0 can be changed to make the system in a relatively ideal state that the Z-source Diode Clamped inverter has less neutral-point potential offset and output THD with a high voltage gain. In this method, K can be recognized as the neutral-point potential index which works with U_C to decide the shoot-through offset.

4.Conclusion

For Z-source Diode Clamped inverter, this paper analyses the effect of shoot-through state on voltage of C_1 and C_2, then concludes that the diode clamped potential unbalance problem can be improved by adding the upper/lower shoot-through offset. Base on it, an improved SPWM control method with the shoot-through offset has been presented for the Z-source Diode Clamped inverter. This method can improve the diode clamped potential effectively and reduce the THD of the output with a high voltage gain. The Matlab/Simulink simulation results with the added shoot-through offset into the maximum constant boost control method and third-harmonic-injection control method verify the effectiveness of this method.

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