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A Mixed Mode Scan Architecture for Serial and Random Access

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A B S T R A C T

Traditional research for testing VLSI circuits has been confined to the use of serial scan design. Over the years, serial scan design has become the de-facto design for testability techniques. Serial scan design has dominated the test architecture because it is convenient to build. In serial scan design existing scan cell eliminates the drawbacks of previous scan cell which was delay due to the scan multiplexers added to the inputs of every flip-flop. However, the serial scan design causes unnecessary switching activity during testing which induces unnecessarily enormous power dissipation. The existing scan cell design used as a common scan flip-flop in the "mixed scan" test where it can be used as a serial scan cell as well as a random access scan (RAS) cell. In this work a new mixed mode scan design architecture adopt both serial and random operations in single module that propose changes in RAS cell where serial data communication internally has series connection of scan cells, to receive the data in series and random methods from every scan cells. It increases the performance in terms of switching activity and power consumption compared to existing mixed mode scan architecture. The experimental results show a promising reduction in total area, power consumption, and delay.

Keywords: Scan Flip-Flop, Scan Design, Serial Scan, Random Access Scan, Mixed Mode Scan

1. Introduction

The advancement ofVLSI technology,ever increasing transistor count in a single chip made them incredibly hard to test. Due to less controllability and observabilityof the storage elements to achieve good fault coverage without Design for Testability (DFT) techniques are impractical. By using DFT techniques it is easier to test the complex designs. In this technique there are two categories were Ad-hoc DFT methods and Structural DFT methods. In these Ad-hoc DFThaving some drawbacks it cannot generate high fault coverage and it is not used for high complex designs. Structured DFT method is alternative for ad-hoc DFT methods. In this design methodology scan design is very important and its playsa crucial role in testing digital circuits by improving controllability and observability of storage elements in the sequential design.

In Scan designthere are two distinct types are Full Scan Design and Partial Scan Design where the full scan design is one type, where all the storage elements are converted into scan flip-flop. A scan flip-flop is Muxed input with D- flip-flop(edge-triggered). The multiplexer uses a Test Enable (TE) input to Select between the Data Input (DI) and the Scan Input (SI).In normal mode of operation, TE is set to 0. The value present at the Data Input (DI) is captured into the internal D flip-flop. When TE is set to 1, the value present in Scan Input is applied to the input of D flip-flop. The advantage of using Muxed-D scan cells are compatibility for modern designs using single clock D flip-flops. But the major disadvantageis each scan cell adds a multiplexer delay to the functional path and each multiplexer delay is equal to two gate delays.

In partial scan design technique only a subset of storage elements in the design are replaced with scan flip-flops to form a scan chain, but it gives less controllability and observability. Serial scan design is one of the mostly used DFT scan design in industries because of its ease of testing and it will take less area. In serial scan design all the scan flip-flops are connected serially to shift the data (Serial shift register).serial scan design using muxed–D scan cell produce additional delay in the functional path and more power consumption [1],[2].To eliminate this penalties a new scan flip-flop designis

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introduced using this scan cell reduces the delay and power consumption and it is also used as a random access scan(RAS) cell in a mixed scan test architecture. Newly, the mixed mode scantest has gained attention by the test community which tries to exploit the best of both serial scan and RAS based DFT techniques [20].

2. Related Work

The design of scancell which is used in mixed mode scan architecture is shown in fig 1. In serial scan and its variations apply a test vector by scan-shifting which creates unnecessary switching activity in the circuit, consuming excessive power. Also each test vector response must be fully shifted in and out of scan chain(s), also a scan cells have to be updatedthroughout test application due to small changes in test vectors.Random-access scan is an alternative DFT technique that can reduce the problems associated with the serial scan design. The implementationof scan function in random-access scan is similar to that of Random-access memory (RAM).

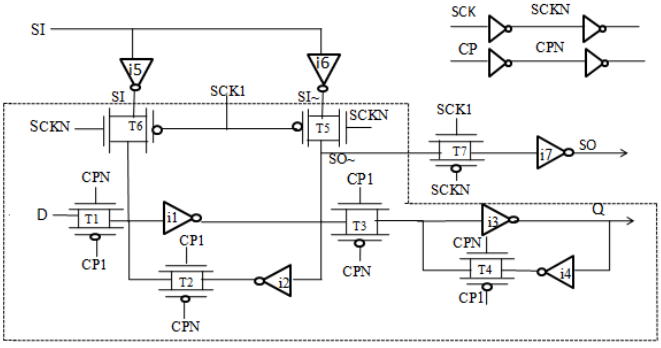

Fig.1 Scan cell design

In RAS, only one input-output is loaded with test stimuli at a time without creating any toggles in other input-outputs. So in RAS power consumption is less comparison to the standard serial scan architecture.RAS architecture is highly power efficient compared to serial scan. As well as the hardware overhead with RAS is high. The practical implementation of Random access scan is impractical due to routing congestion is a serious issue. After that recently,Baik and saluja[4],[5] made some innovative changes to the basic RAS scan architecture to overcome routing congestion issue,and proposed a progressiverandom access scan (PRAS) as shown in fig 2., which access eachscan cell individually. Soit eliminatesunnecessary switching activity during scan by providing such accessibility to every storage cell. A row enable shift register is used to address eachrow one at a time and parallelreading of response and hence minimized the test time. Inmixed mode scan architecture the PRAS is used alongside the standard multiple sequentialscan.

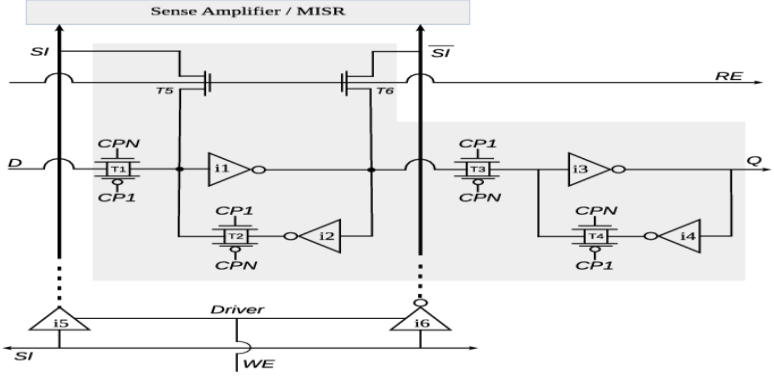

Fig.2 PRAS scan cell

3. Existing Design

This section explores the use of the common scan flip-flop to implement mixed mode scan architecture.The Mixed mode scan design proposed by tudu [6], referred as joint scan hasmixed mode scan architecture with mainly three important components: Multiple Serial Scan (MSS) part, random access scan (RAS) part, and the test controller. The multiple serial scan part is indicated by p-serial, and RAS part is signified by p-random. In mixed mode scan design Both the serial scan test architecture and RAS test architecture implemented using common scan cell shown in fig 1.

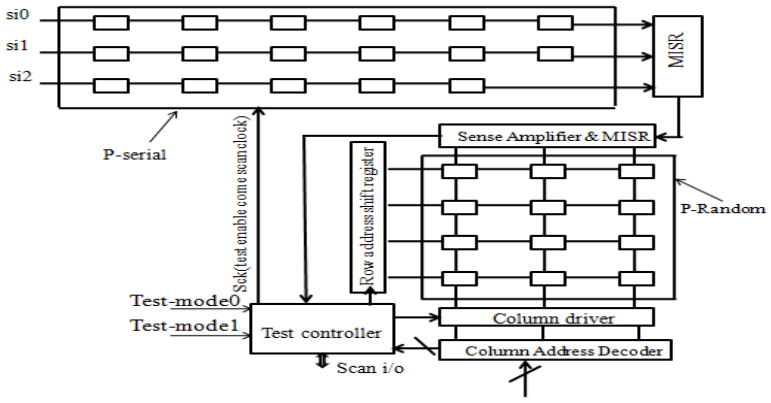

Fig. 3 Mixed mode scan design architecture

The multiple serial scan part isdenoted by p-serial, and RAS part is denoted by p-random. Thep-serialpart consists multiple serial scan chains with inputsSI0, SI1, and SI2, and a MISRat the outputs to compact thetest responses. The number of scan chains can vary dependingupon the available number of test pins. The shift operationin p-serialis performed by using the scan enablecum scanclock signal SCK. The RAS part is denoted by p-randomandimplemented as PRASarchitecture [4]. The row address shiftregister and column driver are used for writing test data. Basedon the column address the test controller generates control signalsto drive the bit and bit-barlines using the column driver.The Sense Amplifierand MISRblock are used to read andcompact the test response data. The MISRfor p-serialandp-randomare connected serially with the controller to shiftout the test response signature via the scan I/O port. The twoinput signals test-mode0and test-mode1 connected to the testcontroller are used to operate the circuitbetween functionalmode and the test mode and exercising the test. The functionality of the circuit is controlled by the two test mode control signals test-mode0and test-mode1. Depending upon the states of the test control signals the circuit can operate in four modes. When both signals are 0, the circuit operates in normal functional mode. The remaining three states are mixed-mode (01), p-random-mode(10), and P-serial mode(11).

4. Implemented work

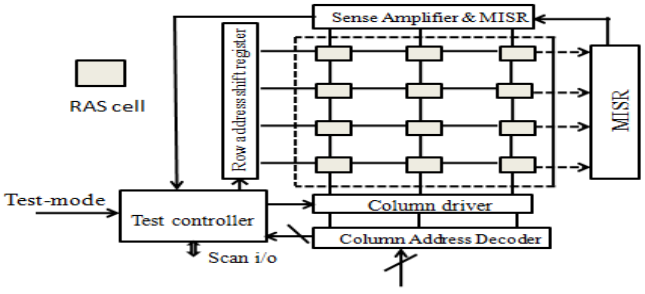

Fig. 4 Implemented Mixed mode scan design architecture

In thisproposed work implementing a design which is in scan chain architecture with efficient performance parameters in terms of area and delay. The implementing design have only one module of scan cells called random access scan cells which are used for both serial and random scan operations , where in existing technique we have two modules one is for multiple serial scan and one is for random access scan test thus it consumes more area and test time. To adopt both serial and random operations in singlemodule form changes to RAS cell where we have serial datacommunication internally with series connection of scan cells, receive the data in series way and random way from every scan cells. The implemented Mixed mode scan design architecture as shown in fig. 4.

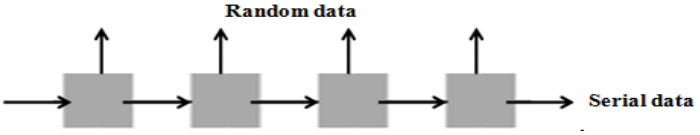

Fig.5 Data processing

The scan cell used for both serial and random access scan design is shown in fig. 1.Scan cell nothing as scan flip-flop. Scan flip-flop works as a regular flip-flop in functional mode. In functional mode, scan clock signal SCK is kept at constant logic high (1) level. As long as SCK is at constant high (1) level the transmission gate T5, and T6 remain disabled. This disconnects the test input path from the master structure and the proposed scan flip-flop functions as a regular flip-flop. The scan clock signal (SCK) held at constant high (1) level indicates functional mode operation. During the functional mode operation, the transmission gate T7 always remains enabled. This keeps the dynamic slave latch always transparent during the functional mode and makes the scan output (SO) toggle every time whenever there is a change in master latch's state. The scan input path remains disconnected from the master structure during the functional mode of operation. The toggling of scan output S0will create switching activity in the scan path which also happens in the conventional scan design.

While keeping the functional clock CPheld at constant high (1) level,scan clock SCK makes the proposed scan flip-flop to functionin test mode. As the functional clock CP is kept high(1), the transmission gate T1 always remains disabled in testmode. This disconnects the functional input D from the masterlatch. During test mode, the master latch gets its inputfrom scan_input SI. The consecutive application of scan clockSCK loads the test values into the scan flip-flops. As it can beobserved in Figure 3, when SCK gets to logic low (0), T5 andT6 get enabled, and the value of SI is written into the masterlatch in a similar way to memory write operation.It should be noted that in test mode since CP is always high(1), the feedback path transmission gate T2 always remainsenabled. This makes the master latch always trying to retainits previous value. However, it can be observed from Figure 3,the test mode input path circuit force writes the SI value simultaneouslyat both input and output nodes of inverter i1 viabuffer i5 and inverter i6 respectively. This makes the writeoperation faster as far as logical fighting is concerned. Whenthe scan clock SCK gets high (1), the dynamic slave latchtransmission gate T7 gets enabled, and the master latch startsdriving both dynamic slave latch inverter i7, and functionalslave latch inverter i3. This propagates the test value latchedinto the master during the negative clock cycle, to dynamicslave latch, and to scan_output SO of the scan cell.

In P-random module the scan cells are connected in bidirectional way, using both serial and random access scan cells for serial scan design .In P-Random that can access any scan cell in any instant by using row address shift register and column address decoder.In proposed design The test controller uses only one test mode pin where as existing Mixedmode Scan uses two test pins. The controller now does not need to keep track of completion of load/unload operation in either P-Serial or P-random unlike in existing mixedmodeScan.This reduces additional circuitry. The proposed controller have only two states: test (Qt) and functional (Qf) (shown in Fig. 6). This saving of one additional pin contribute in minimization of time.

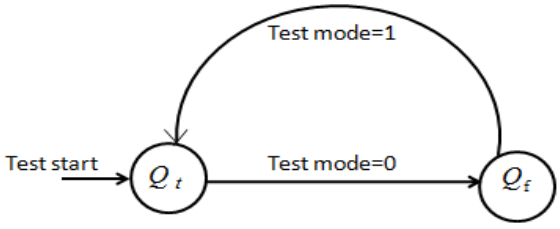

Fig. 6 Test controller mechanism

Functional Mode : The functional mode controls two primary operations: 1.) normal function, and 2.) response capture. Normal function is when the circuit perform desired functional operation in normal mode. row address shift registerand column driver are disabled to operate P-random scan input-outputs as regular input-outputs as well as a serial scan input-outputs as regular input-outputs.Response capture is part of test procedure performed in functional mode. Once thetest stimuli is launched the mode of operation is changed to functional mode (test mode =0), and after a delay of one or more clock cycles (called dead cycles) the response is captured by applying a functional clock pulse.

Test Mode: The test mode is enabled by holding test mode = 1.Test mode controls three primary test operations: 1.) loading/unloading of stimuli/response, 2.) Capturing of stimuli, and 3.) shift out of response from MISR. The row address shiftregister and column driver are used for writing test data. Basedon the column address the test controller generates control signalsto drive the bit and bit-barlines using the column driver.The Sense Amplifierand MISRblock are used to read andcompact the test response data. The test stimuli are scanned in through scan-in lines and responses are compacted usingMISR. The load/unload operation in P-random are performed row by row. First a rowis enabled by signal generated from row address shift register, then the column driveractivates the desired input-outputs in enabled row for to write test stimuli bit one by one.Once a row is completed the same procedure is repeated for next row until the last row. Once load/unloadis completed the test stimuli is launched and test mode is changed to functional mode(test mode = 0) for capture. Once all the test sets are applied and responses are compacted in MISRs the compacted response is shifted out for comparison. This completes entire test procedure.

5. Simulation Results

In this Proposed work i.e., implemented mixed mode scan design architecture is simulated in Incisive Enterprise simulator. The RTL schematic diagram of implemented Mixed mode scan design architecture as show in fig. 7.

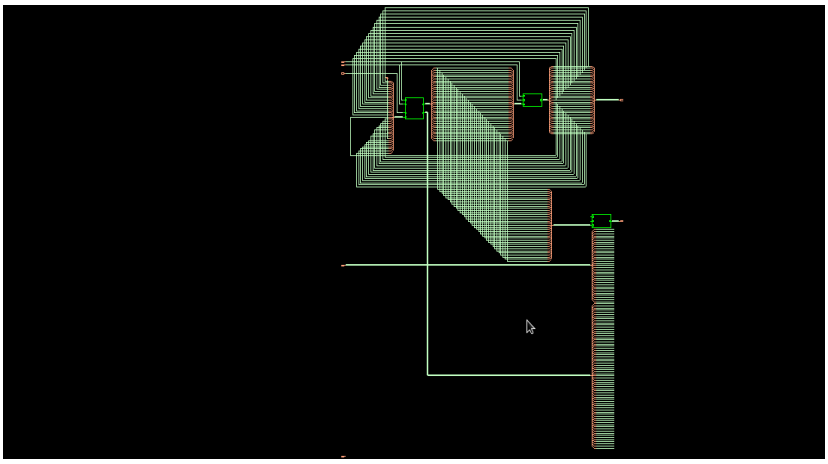

Fig.7 RTL Schematic of implemented mixed mode scan design

RTL Schematic of RAS scan design using scan flip-flops shown in below figure.

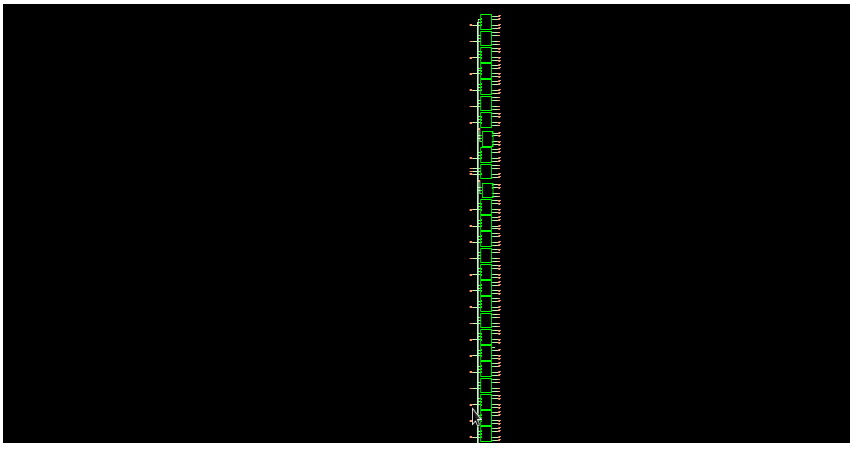

Fig.8 RTL Schematic of RAS design

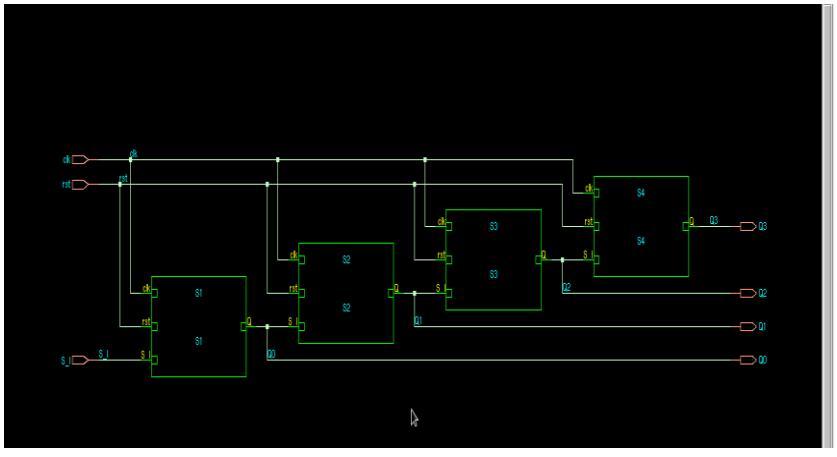

Fig.9 RTL Schematic of single RAS cell

Multiple input signature register (MISR) used to read and compact the test response data. MISR for serial and random are connected serially to testcontroller to shift out the test response signature via scan I/O port.

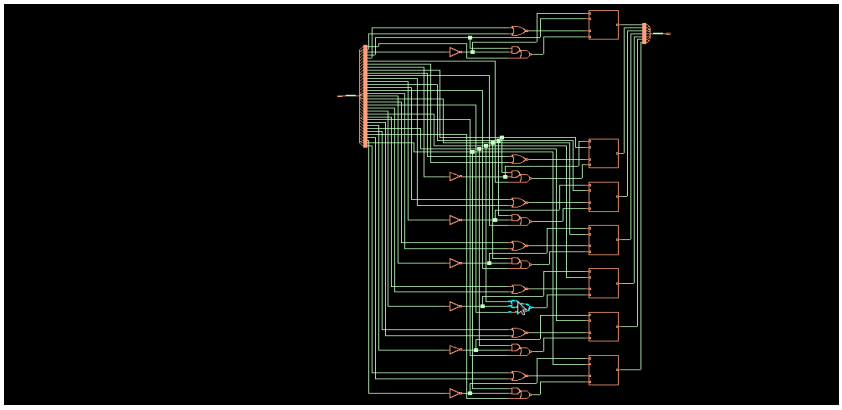

Fig.10 RTL Schematic of MISR

The simulation results of the proposed mixed mode scan design architecture as shown in fig.11

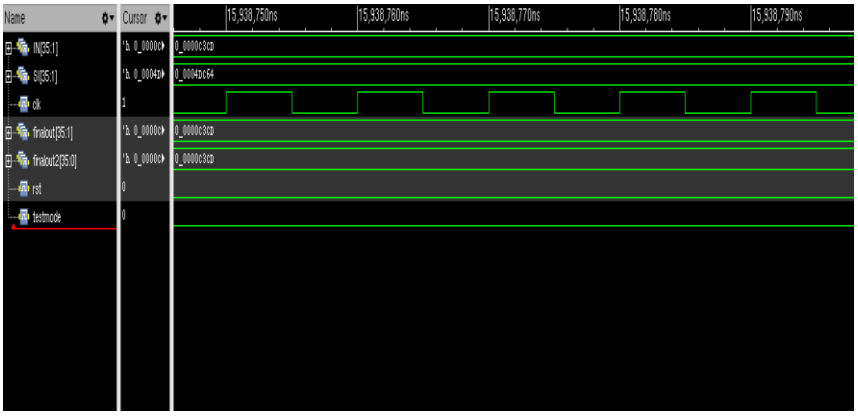

Fig. 11Simulation results of the proposed Mixed mode scan design architecture

Comparison:

The Synthesis results of implemented mixed mode scan designand existing mixed mode scan design acquired using RTL compiler (Cadence) using 90nm technology and clock frequency of 100 MHZ. There is 16% reduction of cells, 17% reduction in total area and 20% reduction in total power with respect to the existing system. To validate the efficiency of the implemented Mixed mode scan design architecture, S5378 bench mark circuit used .

Table I Comparison Of Area and Power

Architecture name	Gate count	Total area(μm^2)	Total Power (nW)
Existing Mixed mode scan design	4246	34735	15836704.051
Implemented Mixed mode scan design	2624	24518	11326212.986

Table II Comparison of Area and Power

Architecture name	Gate count	Total area (μm^2)	Total Power (nW)
Existing Mixed mode scan design using S5378	5117	39631	17675831.437
Implemented Mixed mode scan design using S5378	3636	30401	15925691.191

6. Conclusion

The new mixed mode scan design architecture is capable of accessing data in series method and random method using RAS design which eliminates performance penalty of the existing mixed mode scan design architecture. It increases the performance in terms ofswitching activity andpower consumption compared to existing mixed mode scan architecture

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